CLAIMS

What is claimed is:

1. A computer-implemented method of reducing temperature variation among integrated circuits during burn-in testing, said method comprising:

measuring power consumed by an integrated circuit under test;

measuring an ambient temperature associated with said integrated circuit under test; and

adjusting a body bias voltage of said integrated circuit under test to achieve a desired junction temperature of said integrated circuit under test.

2. The method of Claim 1 wherein said ambient temperature is measured for a region comprising only said integrated circuit under test.

3. The method of Claim 1 wherein said ambient temperature is measured for a region comprising more than one integrated circuits under test.

4. The method of Claim 1 wherein said measuring power comprises measuring current to said integrated circuit under test.

5. The method of Claim 1 wherein an operating voltage of said integrated circuit under test remains fixed during said measuring and said adjusting.

6. The method of Claim 1 wherein said body bias voltage is individually controllable for said integrated circuit under test.

7. The method of Claim 1 wherein said integrated circuit under test comprises body-biasing well structures to accept said body bias voltage.

8. A computer-implemented method of reducing temperature variation among integrated circuits during burn-in testing, said method comprising:

accessing a measurement of power consumed by an integrated circuit under test;

accessing a measurement of an ambient temperature associated with said integrated circuit under test; and

adjusting a body bias voltage of said integrated circuit under test to achieve a desired junction temperature of said integrated circuit under test.

9. The method of Claim 8 wherein said ambient temperature is measured for a region comprising only said integrated circuit under test.

10. The method of Claim 8 wherein said ambient temperature is measured for a region comprising more than one integrated circuits under test.

11. The method of Claim 8 wherein said measuring power comprises measuring current to said integrated circuit under test.

12. The method of Claim 8 wherein an operating voltage of said integrated circuit under test remains fixed during said measuring and said adjusting.

13. The method of Claim 8 wherein said body bias voltage is individually controllable for said integrated circuit under test.

14. The method of Claim 8 wherein said integrated circuit under test comprises body-biasing well structures to accept said body bias voltage.

15. A computer implemented method of determining a junction temperature of an integrated circuit, said method comprising:

measuring an ambient temperature in a region proximate to said integrated circuit;

measuring electrical power utilized by said integrated circuit;

accessing a thermal resistance value for said integrated circuit; and

determining a junction temperature of said integrated circuit.

16. The method of Claim 15 wherein said determining comprises multiplying said thermal resistance value by said electrical power and adding said ambient temperature.

17. The method of Claim 15 wherein said measuring electrical power comprises measuring current to said integrated circuit.

18. The method of Claim 15 wherein said thermal resistance value is accessed from a computer usable media.

19. A system for testing an integrated circuit comprising:

an operating voltage supply for coupling said integrated circuit;

a current measuring device for coupling said integrated circuit for measuring operating current of said integrated circuit;

a body bias voltage supply for coupling said integrated circuit for providing a body bias voltage;

an ambient temperature sensor for determining an ambient temperature for a region proximate to said integrated circuit;

a test controller for coupling said integrated circuit and coupling said current measuring device, said bias voltage supply and said ambient temperature sensor, said test controller for implementing a method for reducing temperature variation among an integrated circuit during burn-in testing, said method comprising:

accessing a measure of power consumed by said integrated circuit;

accessing a measure of ambient temperature associated with said integrated circuit; and

adjusting said body bias voltage of said integrated circuit to achieve a desired junction temperature of said integrated circuit.

20. The system of Claim 19 wherein said ambient temperature is measured for a region comprising only said integrated circuit.

21. The system of Claim 19 wherein said ambient temperature is measured for a region comprising more than one integrated circuits under test.

22. The system of Claim 19 said accessing a measure of power accessing a measure of current to said integrated circuit.

23. The system of Claim 19 wherein an operating voltage of said integrated circuit is fixed.

24. The system of Claim 19 wherein said body bias voltage is individually controllable for said integrated circuit.

25. The system of Claim 19 wherein said integrated circuit comprises body-biasing well structures to accept said body bias voltage.

26. The system of Claim 19 wherein said method implemented by said test controller also comprises stimulating said integrated circuit for testing.

27. A computer usable media comprising computer usable instructions which when executed on a processor implement a method for reducing temperature variation among integrated circuits during burn-in testing, said method comprising:

measuring power consumed by said integrated circuit under test;

measuring an ambient temperature associated with said integrated circuit; and

adjusting said body bias voltage of said integrated circuit to achieve a desired junction temperature of said integrated circuit.

28. The media of Claim 27 wherein said ambient temperature is measured for a region comprising only said integrated circuit.

29. The media of Claim 27 wherein said ambient temperature is measured for a region comprising more than one integrated circuits under test.

30. The media of Claim 27 wherein said measuring power comprises measuring current to said integrated circuit.

31. The media of Claim 27 wherein an operating voltage of said integrated circuit is fixed.

32. The media of Claim 27 wherein said body bias voltage is individually controllable for said integrated circuit.

33. The media of Claim 27 wherein said integrated circuit comprises body-biasing well structures to accept said body bias voltage.